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APPLICATION NO		FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/645,987	08/22/2003		Tirthankar Lahiri	OI7030762001	8636	
23639	7590	06/20/2006		EXAM	EXAMINER	
		UTCHEN LLP	ELMORE, REBA I			
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Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)				
		10/645,987	LAHIRI ET AL.				
	Office Action Summary	Examiner	Art Unit				
		Reba I. Elmore	2189				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
WHIC - Exter after - If NO - Failu Any I	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DATES and the may be available under the provisions of 37 CFR 1.13 SIX (6) MONTHS from the mailing date of this communication. In period for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute, reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 16(a). In no event, however, may a reply be tim rill apply and will expire SIX (6) MONTHS from to cause the application to become ABANDONED	l. ely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status							
· ·	Responsive to communication(s) filed on <u>10 April 2006</u> . This action is FINAL . 2b) This action is non-final.						
3)□	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.						
Dispositi	on of Claims						
5)□ 6)⊠ 7)□ 8)□ Applicati	Claim(s) 1 and 3-40 is/are pending in the application (s) is/are withdraw Claim(s) is/are allowed. Claim(s) 1 and 3-40 is/are rejected. Claim(s) is/are objected to. Claim(s) is/are objected to. Claim(s) are subject to restriction and/or on Papers The specification is objected to by the Examiner The drawing(s) filed on is/are: a) acceed Applicant may not request that any objection to the drawing sheet(s) including the correction is claim (s) is/are: a) acceed to the correction of the drawing sheet(s) including the correct	vn from consideration. relection requirement. r. epted or b)□ objected to by the Edrawing(s) be held in abeyance. See	37 CFR 1.85(a).				
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
Priority u	nder 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 							
2) Notice	(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) nation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) No(s)/Mail Date 4/20/06	4) Interview Summary (Paper No(s)/Mail Dat 5) Notice of Informal Pa 6) Other:	e				

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DETAILED ACTION

1. Claims 1 and 3-40 are presented for examination.

DRAWINGS

2. The objection to the drawings is *withdrawn* due to the amendment.

SPECIFICATION

- 3. The objection to the disclosure is *withdrawn* due to the amendment.
- 4. The objection to the abstract of the disclosure is *withdrawn* due to the amendment.
- 5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

CLAIM OBJECTIONS

6. The objection to claim 3 is objected to as having a spelling or typographical error is withdrawn due to the amendment.

35 USC § 101

- 7. The rejection of 31 under 35 USC § 101 is *maintained* and repeated below. Newly added claims 32-40 are added to this non-statutory rejection under 35 USC § 101.
- 8. 35 USC § 101 reads as follows:
 - Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.
- 9. Claims 31-40 are rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter. This interpretation is based on the following reasoning:

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Claims 31-40 are not limited to tangible embodiments. In view of the Applicant's disclosure, specification page 15, paragraph 0045, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., ROM 409, CD ROM, magnetic tape, magnetic discs, main memory) and intangible embodiments (e.g., transmission medium). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

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10. Additionally, the language of claim 31 raises a question of including inoperative claim limitations. Claim 31 is rejected under 35 USC § 101 because the disclosed invention is inoperative and therefore lacks utility.

Claim 31 now states using 'computer usable storage medium', however, the specification does not define 'storage medium' just 'computer-usable medium' and 'computer-readable medium' which the specification, page 15, paragraph 0045, defines as including 'transmission media'. A computer usable medium, such as that claimed, must have the capability of storing data for execution by a computer or processing system. Transmission media cannot be used to store the executable code for use in the system. Coaxial cable, copper wire, fiber optics, carrier waves and electromagnetic waves provide connectivity within the system but it is a misuse of the terminology in the memory art to imply these elements also 'store' data without further teaching how to make and use these elements in such a way.

35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

- 12. Claims 1, 3-7, 12-13, 15, 19, 21-24, 28-29, 31-34 and 38-40 are rejected under 35 U.S.C. 102(e) as being anticipated by Herbst et al. (P/N 6,907,499)
- 13. Herbst teaches the invention (claim 1) as claimed including a method for reducing input/output operations (IOs) by coalescing writes in a computer system, the computer system comprising:

identifying, in a first storage location, a first data block to be written into a second storage location, the first data block having a first data block address as a first data block stored in the write cache (e.g., see col. 2, lines 25-40);

identifying, in the first storage location, additional data blocks to be written into the second storage location as identifying disc contiguous data block (e.g., see col. 2, lines 25-40);

tracking a total number of the identified first and additional data blocks as using the ROSI algorithm which determines the last data sector to which data is to be written (e.g., see col. 8, line 17 to col. 9, line 44 and col. 13, lines 11-65); and,

writing the identified first and additional data blocks to the second storage location with a write operation, in which the first and additional data blocks comprising a set of data blocks with consecutive block addresses as identifying contiguous data blocks (e.g., see col. 2, lines 25-40).

As to claim 3, Herbst teaches setting a predetermined upper limit for the total number of the identified first and additional data blocks, in which if the predetermined upper limit is met by the total number of the identified first and additional data blocks, the method stops identifying additional data blocks and immediately writes the identified first and additional data blocks to the second storage location as the computer system using a write cache memory which has a finite number of locations for temporary storage. Once the cache is filled, data must be written back to the disc. This feature is an inherent capability of a cache memory.

As to claim 4, Herbst teaches copying each of the identified first and additional data blocks to a temporary storage location, wherein writing the identified first and additional data blocks to the second storage location is accomplished by writing copies of the identified first and additional data blocks in the temporary storage location to the second storage location as using a write cache (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 5, Herbst teaches marking the identified first and additional data blocks in the first storage location not dirty each time after an identified data block is copied to the temporary storage location as doing a read back of the data element which would eliminate the dirty status of the block (e.g., see col. 5, lines 21-37).

As to claim 6, Herbst teaches the temporary storage location is a temporary buffer cache (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 7, Herbst teaches sequentially searching the first storage location to identify next data blocks with higher or lower data block addresses consecutive to the first data block address as determining whether or not there is uncommitted data waiting to be written to the disc (e.g., see col. 6, line 56 to col. 7, line 17);

determining whether an identified next data block is dirty with the determination as to whether there is uncommitted data waiting to be written to the disc (e.g., see col. 6, line 56 to col. 7, line 17); and,

wherein if the identified next data block is not dirty, the method stops sequentially searching for new data blocks with data block addresses at a same data block address side to the data block addresses of the identified next data block (e.g., see col. 6, line 56 to col. 7, line 17).

As to claim 12, Herbst teaches the first storage location is a buffer cache (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 13, Herbst teaches the second storage location is a disk (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 15, Herbst teaches copying the first and additional data blocks to form a copy of the first and additional data blocks and allowing other entities in the computer system to access the copy of the first and additional data blocks during the act of writing the first and additional data blocks (e.g., see col. 7, line 45 to col. 8, line 6).

As to claim 19, Herbst teaches the first storage location is a buffer cache, wherein the entire buffer cache is search (e.g., see col. 5, line 57 to col. 6, line 11).

14. Herbst teaches the invention (claim 21) as claimed including a computer system comprising:

means for identifying, in a first storage means, a first data block to be written into a second storage location, the first data block having a first data block address as a first data block to be stored in the write cache (e.g., see 2, line 25-40);

means for identifying, in the first storage means, an additional data block to be written into the second storage location (e.g., see col. 7, lines 18-32);

means for tracking a total number of the identified first and additional data blocks as using the ROSI algorithm which determines the last data sector to which data is to be written (e.g., see col. 8, line 17 to col. 9, line 44 and col. 13, lines 11-65); and,

means for writing the identified first and additional data blocks to the second storage means with a single write IO, in which the first and additional data blocks comprise a set of data blocks with consecutive data block addresses as multiple write commands which identify either consecutive addresses or additional address (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 22, Herbst teaches a means for setting a predetermined upper limit of the total number of the identified first and additional data block, in which if the predetermined upper limit is met by the total number of the tracking means, the computer system stops identifying additional data blocks and immediately writes the identified first and additional data blocks to the second storage means as there being a size of the block of data which is an inherent capability of a memory system. The system uses this as an amount of data for moving the data from one part of the system to another.

As to claim 23, Herbst teaches a temporary storage means for temporarily storage data in a third plurality of data blocks as the write cache which has a plurality of temporary storage for data block, means for copying each of the identified first and additional data blocks to a temporary storage means, means for marking one of the identified first and additional data blocks in the first storage means not dirty after the identified first and additional data blocks is copied to the temporary storage means, in which the identified first and additional data blocks are written to the second storage means by copying the identified first and additional data blocks

in the temporary storage means to the second storage means (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 24, Herbst teaches the temporary storage means is a temporary buffer cache (e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 28, Herbst teaches the first storage means is a buffer cache(e.g., see col. 5, line 57 to col. 6, line 11).

As to claim 29, Herbst teaches the second storage means is a disk (e.g., see col. 5, lines 6-37).

15. Herbst teaches the invention (claim 31) as claimed including a computer program product comprising a computer usable medium having executable code to execute a process for reducing IOs by coalescing writes in a computer system, the process comprising:

identifying, in a first storage location, a first data block ready to be written into a second storage location, the first data block having a first data block address as a first data block stored in the write cache (e.g., see col. 2, lines 25-40);

identifying, in the first storage location, additional data blocks to be written into the second storage location as identifying disc contiguous data blocks (e.g., see col. 2, lines 25-40);

tracking a total number of the identified first and additional data blocks as using the ROSI algorithm which determines the last data sector to which data is to be written (e.g., see col. 8, line 17 to col. 9, line 44 and col. 13, lines 11-65); and,

writing the identified first and additional data blocks to the second storage location with a single write IO, in which the first data block and the additional data blocks form a set of data

blocks with consecutive data block addresses (e.g., see col. 2, lines 25-40 and col. 5, line 57 to col. 6, line 11).

As to claim 32, Herbst teaches the process for reducing IOs further comprises setting a predetermined upper limit of the total number of the identified first and additional data blocks, in which if the predetermined upper limit is met by the total number of the tracking means, the computer system stops identifying additional data blocks and writes the identified first and additional data blocks to the second storage location (e.g., see col. 2, lines 25-40 and col. 5, line 57 to col. 6, line 11).

As to claim 33, Herbst teaches the process for reducing IOs further comprises temporarily storing data on more data blocks, copying each of the identified first and additional data blocks to a temporary storage location and marking one of the identified first or additional data blocks in the first storage location not dirty after the identified first or additional data block is copied to a temporary storage location, in which the identified first and additional data blocks are written to the second storage location by copying the first and additional data block in the temporary location to the second storage location as using a write cache to temporarily store data to be copied to the disc (e.g., see Figures 2-3 and col. 6, line 56 to col. 7, line 32).

As to claim 34, Herbst teaches a computer usable storage medium having an executable code to execute a process for reducing IOs, in which one or more data blocks are stored in a temporary buffer cache as having a write cache and coalescing write operations (e.g., see col. 2, lines 15-49).

As to claim 38, Herbst teaches the first storage is a buffer cache (e.g., see Figure 2).

As to claim 39, Herbst teaches the second storage is a disk (e.g., see Figure 2).

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As to claim 40, Herbst teaches the computer is a database system (e.g., see col. 5,-lines 22-36).

35 USC § 103

- 16. The rejection of claims 8-11, 14, 16-18, 20, 25-27 and 30 as being unpatentable over Herbst et al. is *maintained* and repeated below with the inclusion of support for the official notice citation. Claims 35-37 have been added to this rejection.
- 17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 18. Claims 8-11, 14, 16-18, 20, 25-27, 30 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herbst et al.
- 19. Herbst teaches the limitations of the independent claims and intervening claims as given above.
- 20. As to claims 8-11, 16-17, 25-27 and 35-37, Herbst does not specifically teaches sequentially searching the first storage location is conducted alternatively at the lower and higher data block address sides to the first data block address, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to search for both lower addresses and upper addresses consecutive to the temporarily stored block addresses and official notice is taken thereof. Herbst does teach data requests from the disc tend to be in a sequential or predictably ordered manner. Additionally, and in support of the official notice, the Gaertner et

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al. ()P/N 6,339,811) reference specifically teaches prefetching RLA (read look ahead) data and ZLP (zero latency prefetching) data as prefetching data immediately ahead of the target data and prefetching data rotationally positioned behind the target or requested data. This is equivalent to the lower and higher data block address sides. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gaertner with the teachings of Herbst as the Gaertner reference is incorporated by reference to the Herbst reference.

- As to claims 14, 18 and 30, Herbst does not specifically teach the computer system is a database system, however, a database system is merely the organization of the stored data. The present invention has not been claimed giving the organization of the data specific importance. It would have been obvious to one of ordinary skill in the memory art at the time the invention was made to establish the stored data in a database system format and official notice is taken thereof.
- As to claim 20, Herbst does not specifically teach searching the entire cache buffer using a hashing operation,, however, the Applicant's specification does not teach or show how the searching is performed using hashing. This limitation appears to be a nominal recitation directed toward the typical hashing used for performing address searching. It would have been obvious to one of ordinary skill in the memory art at the time the invention was made to utilize a hashing algorithm to search the entire write cache and official notice is taken thereof.

RESPONSE TO APPLICANT'S REMARKS

23. Applicant's arguments filed April 10, 2006 have been fully considered but they are not persuasive.

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24. As to the reference not teaching 'tracking a total number of the identified first and additional data blocks', this limitation is taught to the extent required by the actual claim language. Herbst specifically teaches being able to determine whether a disc write operation is 'in progress' and whether on not the write operation should be aborted or interrupted. The system must have identified the amount of data involved in the write operation in order to determine whether to abort the write operation, interrupt the write operation or let the write operation finish. The data involved in the write operation is identified in order to make the operational flow determination operation.

25. As to the request for support for the official notice, the rejection under 35 USC §103 has been updated to include the supporting reference.

OFFICE ACTION FINALITY

26. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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CONCLUSION

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Tuesday and Thursday from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore

Primary Patent Examiner

Rha P. Elm

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Friday, June 09, 2006